operation unit for performing a butterfly operation at each of the stages according to a radix algorithm, a scale detection unit for calculating and outputting a scale factor which is a division factor used for controlling a bit value of a butterfly operated signal input from the butterfly operation unit at each of the stages to a predetermined bit limit of the received OFDM signal, a scale count unit for cumulative counting a count figure corresponding to the scale factor input from the scale detection unit and outputting the result, and a compensation unit for controlling the bit of a signal input from the butterfly operation unit according to result values from the scale detection unit and the scale count unit and outputting the result.

The compensating unit includes a second operation unit for dividing the bit value of the butterfly operated output signal at the final stage of the predetermined stages by the scale factor calculated at the final stage, a division and multiplication selection unit for calculating a difference value of the predetermined number of stages and an output value from the scale count unit, comparing the predetermined number of stages with the output value from the scale count unit and outputting a selection signal for division operation if the predetermined number of stages is greater or a selection signal for multiplication if the output value from the scale count unit is greater, a coefficient calculation unit for calculating and outputting a quotient Q and a remainder R by dividing the difference value by 2, a division and multiplication calculation unit for dividing the value output from the second operation unit by 2^Q if the selection signal is for the division operation or

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multiplying the value output from the second operation unit by 2^Q if the selection signal is for the multiplication operation, a bit compensation unit for compensating the value output from the division and multiplication calculation unit according to the selection signal from the division and multiplication selection unit and the remainder **R** from the coefficient calculation unit, and an adder unit for adding the data input from the bit compensation unit and outputting the result.

To achieve the objective of the invention, there is provided a Fast Fourier Transforming method for compensating an OFDM output bit signal, including a step of input buffering for storing and outputting a received OFDM bit signal, a step of first operation for dividing the received signal by a scale factor and outputting the result, a step of butterfly operation for butterfly operating on the result at each of the stages according to a radix algorithm and outputting the butterfly operated signal, a step of scale detection for calculating the scale factor which is a division factor that is used for controlling the bit value of the butterfly operated signal to fall within the predetermined bit limit of the OFDM signal input at the step of the input buffering, a step of scale count for cumulative counting a count figure corresponding to input bit scale factor and outputting the cumulative scale count value, wherein the step of input buffering through the step of a scale count are repeatedly conducted until the scale count value reaches a predetermined number of stages, and a step of compensation for controlling

the butterfly operated value which is calculated at the final stage of the predetermined stages according to the scale factor and the scale count value.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objective and advantage of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIGS. 1A and 1B are flowcharts for showing the conventional method for compensating for an output bit signal;

FIG. 2 is a block diagram illustrating a Fast Fourier transforming apparatus for compensating an OFDM output bit signal according to the present invention;

FIG. 3 is a flowchart for showing the steps of calculating a scale factor in the scale detection unit;

FIG. 4 is a detailed block diagram illustrating a compensation unit of FIG. 2;

FIG. 5 is a flowchart for showing the steps of selecting a division or multiplication of the division and multiplication selection unit of FIG. 4;

FIG. 6 is a flowchart for showing the steps of calculating a coefficient of the coefficient calculation unit of FIG. 4;

FIG. 7 is a flowchart for showing the steps of division or multiplication calculation of division and multiplication calculation unit of FIG. 4; and

FIG.8 is a flowchart for showing the steps of compensating for bit signal of bit compensation unit of FIG. 4.